REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the following remarks. The Applicant originally submitted Claims 1-20 in the application. The Applicant amended Claims 1, 8 and 15 in the Applicant's March 17, 2005, response ("previous response"), but makes no amendments in this response. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 103(a)

The Examiner rejected Claims 1, 3, 6, 7, 8, 10, 13, 14, 15, 17 and 20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,784,603 to Leung, *et al.*, in view of U.S. Patent 4,910,664 to Arizono, *et al.* In the previous response, the Applicant took the position that the combination of Leung and Arizono fails to teach or suggest each and every element of Claims 1, 8 and 15 and therefore fails to support a *prima facie* case of obviousness as M.P.E.P. ¶ 2143 requires. In the June 27, 2005, Examiner's Action ("current Action"), the Examiner sustained the rejection of Claims 1, 8 and 15 over the combination of Leung and Arizono. The Applicant again respectfully traverses the Examiner's rejection.

The Applicant first addresses the Examiner's arguments presented in ¶ 7 of the current Action. The element of Claims 1 and 8 at issue is "a loop recognizer, coupled to said prefetch circuitry, that determines whether a loop is present in fetched instructions and reinstates a validity of said fetched instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution." Claim 15 uses similar language to describe the same element. In the previous response, the Applicant argued:

> First addressing the element of preventing prefetch outside of the loop, the Examiner states in § 9 of the Office Action that Arizono, column 3, lines 10-67 and column 5, lines 43-54 teach, "The prefetch counter is reset to the loop-beginning address each time the prefetch counter equals the loop-ending address, thereby preventing said prefetch circuitry from prefetching instructions outside of said loop until said loop completes processing." However, column 5 line 64 through column 6 line 2, and FIGURE 5, state 4, teach that because the instruction bus is 16 bits wide, a byte fetch may result in the fetch of an additional byte past the end of the loop, which is then discarded when the prefetch counter is reset to the beginning of the loop. Thus, Arizono does not prevent the prefetch circuitry from prefetching instructions "outside of said loop until said loop completes execution," and Arizono fails to teach this limitation.

In the current Action, the Examiner does not dispute the Applicant's argument, but instead directs the Applicant to column 6, lines 40-44, of Arizono, erroneously characterizing the latter passage as teaching the prefetch of only one byte instead of a plurality of bytes, thereby eliminating the fetch of an additional byte past the end of the loop. But this is not what Arizono teaches. Column 6, lines 40-44, instead reads:

> Although the plural bite prefetch is carried out in the above described preferred embodiment, only one *bit* may be prefetched with the same effect as in the above described preferred embodiment.

(Emphasis added.)

Column 6, lines 40-44, clearly teaches prefetching only a single bit. One of ordinary skill in the art would not be motivated to combine the teaching of Leung with prefetching a single bit of an instruction, as no useful instruction information is conveyed by prefetch of a single bit. Thus, there is no motivation to combine Leung and Arizono. Moreover, because prefetch of a single bit conveys no useful information, there is no reasonable expectation of success by combining Leung with the cited teaching. Because there is no motivation to combine Leung and Arizono, and there is no reasonable expectation of success, the cited combination fails to support a *prima facie* case of obviousness of Claims 1, 8 and 15.

While maintaining that Arizono teaches prefetch of *one bit* at column 6, line 40-44, the Applicant recognizes from the Examiner's remarks in the current Action that the Examiner interprets the passage to suggest prefetch of a single *byte* of an instruction sequence. However, such an interpretation is not valid, because Arizono cites the use of "bit" in multiple locations. Without more, the teaching of the cited passage must be taken at face value, and the Examiner's extension is unfounded.

However, even if Arizono does suggest prefetch of a single byte, while maintaining that it does not, there is still no motivation to combine Leung and Arizono. In the June 28, 2004, examiner's action, the Examiner asserted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Leung include the loop recognizer as taught by Arizono. "The test for an implicit showing [of obviousness] is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." (M.P.E.P. ¶ 2143.01.) However, while Leung is directed to quick and efficient handling of mispredicted branch instructions in a computer processor (see Abstract), Arizono is directed to eliminating the need for repeated address calculation for branching to a loop beginning address after each loop execution cycle. (See Abstract.) While both Leung and Arizono are generally directed to computational hardware, the nature of the problems to be solved in each reference are otherwise unrelated. One of ordinary skill in the art attempting to further improve the efficiency of the apparatus of Leung would not look to Arizono for a solution.

Moreover, specific factual findings with respect to the motivation to combine references is required to sustain a *prima facie* case of obviousness. (See M.P.E.P. ¶ 2143.01.) Notwithstanding

the assertion by the Examiner that one of ordinary skill in the art would be motivated to combine Leung and Arizono "for the desirable purpose of avoiding wasteful prefetching" (June 28, 2004, Examiner's Action ¶ 7), the Examiner utterly fails to provide evidence that Leung suffers from inefficiency from prefetching outside of an instruction loop. Without a need to add functionality to prevent prefetching outside of an instruction loop, Leung would have a disincentive to burden a branch predictor with additional hardware. Thus, the Examiner has failed to provide specific factual findings with respect to motivation to combine Leung and Arizono, and their combination is improper.

Next addressing the Examiner's arguments contained in ¶ 8 of the current Action, the Examiner asserts that the Applicant is arguing a feature of the invention not specifically stated in the claim language. The Applicant respectfully disagrees. In the previous response, the Applicant argued

> In reinstating a validity of instructions, at best Arizono teaches the reinstatement of the validity of instructions in the abstract sense, *i.e.*, returning to the top of the loop in the computational algorithm." Distinguishing Arizono from the inventions of Claims 1, 8 and 15, the Applicant continued, "[a]n element of Claims 1, 8 and 15 is the *specific* reinstatement of the validity of instructions residing in the instruction cache to obviate the need to fetch these instructions again ('...reinstates a validity of said fetched instructions...'). Nowhere is this limitation taught or suggested by Arizono.

(Emphasis in original.)

While the Examiner is permitted to interpret the pending claims "as broadly as their terms reasonably allow" (In re Prater, 162 USPQ 541, 550-51 (CCPA 1969)), the Examiner must rely on the applicant's disclosure to properly determine the meaning of the claims (Markman v. Westview Instruments, 34 USPQ2d 1321, 1330 (Fed. Cir.) (*en banc*), aff'd 116 S. Ct. 1384 (1996)). The Specification fully supports the limitation in question at ¶¶ 39, 46 and 47 and FIGURE 4. The

Examiner may have failed to appreciate that in each of Claims 1, 8 and 15, the element "said fetched instructions" has antecedent support from the element "fetched instructions" in the same clause of the claim. Specifically, each of Claims 1, 8 and 15 recites "...fetched instructions and reinstates a validity of *said* fetched instructions..." (emphasis added). While "limitations appearing in the specification will not be read into the claims" (Intervet Am. v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)), elementary principles of claim construction require interpreting "said fetched instructions" to mean those fetched instructions recited earlier in the claim. Therefore, "said fetched instructions" is unambiguous in its meaning.

The Applicant's argument that this element provides for "the specific reinstatement of the validity of instructions residing in the instruction cache to obviate the need to fetch these instructions again" (Applicant's Response, March 17, 2005, at ¶ 8) does not argue a limitation not already present in the Claim. Arizono fails to teach or suggest this limitation, so the combination of Leung and Arizono fails to teach each and every limitation of the invention claimed in Claims 1, 8 and 15, and the Claims are allowable.

For at least these reasons, Arizono fails to cure the deficiency of Leung, and the combination of Leung and Arizono fails to support a *prima facie* case of obviousness. Thus, independent Claims 1, 8 and 15 and those dependent thereon are allowable.

III. Conclusion

In view of the foregoing remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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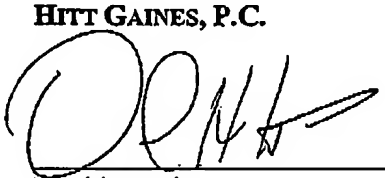

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